



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,843	04/02/2004	Byung Chul Ahn	8733.1047.00-US	9693
30827	7590	06/06/2005	EXAMINER	
MCKENNA LONG & ALDRIDGE LLP			SEFER, AHMED N	
1900 K STREET, NW			ART UNIT	
WASHINGTON, DC 20006			PAPER NUMBER	
			2826	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

22

Office Action Summary	Application No.	Applicant(s)	
	10/815,843	AHN ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 16-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (claims 1-15) in the reply filed on 4/21/2005 is acknowledged.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is insufficient antecedent basis for "the gate insulating film" recited in claim 15.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Byun et al. ("Byun") WO 03/001606.

Byun discloses in figs. 1-11 a liquid crystal display having an applied horizontal electric field comprising: a gate line 22; a common line 27 substantially parallel to the gate line; a data line 62 arranged to cross the gate line and the common line to define a pixel area; a thin film transistor TFT formed at each crossing of the gate line and the data line; a common electrode 28

Art Unit: 2826

formed in the pixel area and connected to the common line; a pixel electrode 68 connected to the thin film transistor, wherein the horizontal electric field is formed between the pixel electrode and the common electrode in the pixel area; a gate pad 24 formed with at least one conductive layer included in the gate line; a data pad 64 formed with at least one conductive layer included in the data line; a common pad 39 formed with at least one conductive layer included in the common line; a passivation film 70 exposing at least one of the gate pad, the data pad and the common pad and a driving integrated circuit mounted on a substrate connected directly to one of the gate pad and the data pad (page 10, lines 27-30).

Regarding claim 13, Byun discloses a thin film transistor comprising: a gate electrode 26 connected to the gate line; a source electrode 65 connected to the data line; a drain electrode 66 opposite the source electrode; and a semiconductor layer 42 for forming a channel portion between the source electrode and the drain electrode.

Regarding claim 14, Byun discloses in fig. 6 the drain electrode and the pixel electrode are made of an identical conductive layer 60.

Regarding claim 15, Byun discloses the semiconductor layer being formed on the gate insulating film 30 along with the data line, the source electrode, the drain electrode and the pixel electrode.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2826

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-3 and 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art (APA) in view of Park et al. ("Park") USPN 6,678,018.

The APA discloses in figs. 1-3 a liquid crystal display having an applied horizontal electric field comprising: a gate line 2; a common line 16 substantially parallel to the gate line; a data line 4 arranged to cross the gate line and the common line to define a pixel area 5; a thin film transistor 6 formed at each crossing of the gate line and the data line; a common electrode 18 formed in the pixel area and connected to the common line; a pixel electrode 14 connected to the thin film transistor, wherein the horizontal electric field is formed between the pixel electrode and the common electrode in the pixel area; a gate pad 24 formed with at least one conductive layer included in the gate line; a data pad 30 formed with at least one conductive layer included in the data line; a common pad 36 formed with at least one conductive layer included in the common line; a passivation film 52; and a driving integrated circuit mounted on a substrate connected directly to one of the gate pad and the data pad (pars. 0020-0021); but lacks anticipation of a passivation film exposing at least one of the gate pad, the data pad and the common pad.

Park discloses (see fig. 5 and col. 7, lines 58-65) a liquid crystal display having an applied horizontal electric field including a data pad 64 and a gate pad 23 and a passivation film 70 exposing at least one of the gate pad, the data pad.

Since the APA and Park are both from the same field of endeavor, LCD device, Park's teachings would have been recognized in APA's pertinent art. Therefore, in view of Park's teachings, one having an ordinary skill in the art at the time the invention was made would be

Art Unit: 2826

motivated to modify APA's device by incorporating a passivation film exposing at least one of the gate pad, the data pad since that would eliminate the need of a shadow mask to form the pads thereby reducing manufacturing cost as taught by Park.

Regarding claim 2, the APA discloses (pars. 0020-0021) the driving integrated circuit including a gate driving integrated circuit connected to the gate pad (not shown).

Regarding claim 3, the APA discloses (pars. 0020-0021) the driving integrated circuit further includes a data driving integrated circuit connected directly to the data pad.

Regarding claim 5, the APA discloses (par. 0014) a signal supplying line for supplying a driving signal to the driving integrated circuit.

Regarding claim 6, the APA discloses each of the gate line and the common line including a main conductive layer 42 and a secondary conductive layer 44.

Regarding claim 7, the APA discloses each of the gate pad 24 and the common pad 36 comprising the main conductive layer 26/38 and the secondary conductive layer 28/40, and wherein the secondary conductive layer has an exposed structure.

Regarding claim 8, the APA discloses each of the gate pad and the common pad comprising the secondary conductive layer.

Regarding claim 9, the APA discloses the main conductive layer including at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten that are a low resistance metal, wherein the secondary conductive layer includes a titanium.

Regarding claim 10, the APA discloses the data pad 30 comprising a main conductive layer 32 and a secondary conductive layer 34.

Art Unit: 2826

Regarding claim 11, the APA discloses the secondary conductive layer having an exposed structure.

As for the recitation “protecting against an opening of the main conductive layer” of claims 6 and 10, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 12, the APA discloses the main conductive layer including at least one of an aluminum system metal, a copper, a molybdenum, a chrome and a tungsten that are a low resistance metal, wherein the secondary conductive layer includes a titanium.

Regarding claim 13, the APA discloses a thin film transistor comprising: a gate electrode 8 connected to the gate line; a source electrode 10 connected to the data line; a drain electrode 12 opposite the source electrode; and a semiconductor layer 48 for forming a channel portion between the source electrode and the drain electrode.

7. Claims 2 and 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byun in view of Lee et al. (“Lee”) WO 03/036374

Byun discloses the device structure as recited in the claim, but lacks anticipation of data driving integrated circuit connected directly to a data pad.

Art Unit: 2826

Lee discloses in figs. 1-4 a liquid crystal display having an applied horizontal electric field comprising: a gate line 22; a common line 88 substantially parallel to the gate line; and data driving integrated circuit 300 connected directly to a data pad 62.

Since the Byun and Lee are both from the same field of endeavor, LCD device, Lee's teachings would have been recognized in Byun's pertinent art. Therefore, in view of Lee's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Byun's device by incorporating data driving circuit connected directly to a data pad since that would improve aperture ration as taught by Lee.

Regarding claim 2, Lee discloses (page 20, lines 20-23) the driving integrated circuit including a gate driving integrated circuit (not shown) connected to a gate pad 22.

8. Claims 2 and 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byun in view of Komatsu US PG-Pub 2002/0067455

Byun discloses the device structure as recited in the claim, but lacks anticipation of data driving integrated circuit connected directly to a data pad.

Komatsu discloses in figs. 2-6 a liquid crystal display having an applied horizontal electric field comprising: a gate line 101; a common line 103 substantially parallel to the gate line; and data driving circuit 154 connected directly to a data pad 155.

Since the Byun and Komatsu are both from the same field of endeavor, LCD device, Komatsu's teachings would have been recognized in Byun's pertinent art. Therefore, in view of Komatsu's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Byun's device by incorporating data driving circuit connected

Art Unit: 2826

directly to a data pad since that would reduce contacting electric resistance between the pad and the driving circuit as taught by Komatsu.

Regarding claim 2, Komatsu discloses the driving integrated circuit including a gate driving integrated circuit 150 connected to a gate pad 151.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Byun in view of Komatsu as applied to claims 1 and 2 above, and further in view of Chiyabara et al. ("Chiyabara") JP 2003-195784.

The combined references above disclose the device structure as recited in the claim, but lack anticipation of a conductive film.

Chiyabara discloses in figs. 5 and 6 a liquid crystal display including a driving integrated circuit 52 connected to a pad using a conductive film 50.

Therefore, in view of Chiyabara's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify the device by incorporating a conductive film since that would achieve a high reliability as taught by Chiyabara.

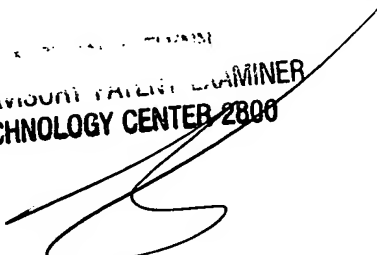
Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Art Unit: 2826

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
May 24, 2005


SUPERVISOR, PATENT EXAMINER
TECHNOLOGY CENTER 2800